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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,047	02/19/2004	Anoop Mukker	42P18617	6837

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EXAMINER	
NGUYEN, DANG T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 12/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/784,047	MUKKER ET AL.	
	Examiner	Art Unit	
	Dang T Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,13,20,32 and 39* is/are rejected.

7)☒ Claim(s) *2–12,14–19,21–31,33–38,and 40–44* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/10/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search history*.

DETAILED ACTION

1. This action is responsive to the following communications: the Application filed on February 19, 2004 and the Information Disclosure Statement filed on September 10, 2004.

2. Claims 1 – 44 are pending in this case. Claims 1, 13, 20, 32, and 39 are independent claims.

Drawings

3. The drawings informalities filed on 02/19/04 are acceptable for examination; formal drawing is required in response to this office action.

Information Disclosure Statement

4. The information disclosure statement filed 9/10/04 has been considered.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 13, 20, 32 and 39 are rejected under 35 U.S.C. 102(b) as being anticipate by Greeff et al., Pub.No.: US 2002/0083255 A1 – Pub. Date: Jun. 27, 2002.

Regarding independent claim 1, Fig. 18 of Greff et al. discloses a method, comprising: by a memory controller [31]: for a first read of information from a memory, activating termination loads (terminal load [452] of Fig. 18 is the same of terminal load [38] of Fig. 1; See Page 2, lines 12 – 14 of paragraph 0032) on said memory controller's side [31] of a data bus [28] between said memory controller [31] and said memory [24, 26]; for a write of information into said memory, deactivating said termination loads ([452]; See Page 2, lines 12 – 14 of paragraph 0032); and, for a second read of information from said memory, activating said termination loads (this is inherent to the method of Greff et al. as discussed above, because Greff et al. taught the terminal loads [452] is activated for each and every read operations. Therefore, the termination loads [452] is activated for second read operation, or third read operation, or fourth read operation and so on).

Regarding independent claim 13, Fig. 18 of Greeff et al. discloses an apparatus, comprising: a memory controller [31] comprising a data bus termination loads [452], said data bus to couple to a memory [24, 26], said termination loads coupled to an output of memory controller logic circuitry [28, 39], said memory controller logic circuitry [31] to drive said output to place said termination loads in an activated state during a memory read phase and to place said termination loads in a deactivated state during a memory write phase (See Page 2, lines 12 – 14 of paragraph 0032).

Regarding independent claim 20, Greff et al. discloses a method, comprising: by a computing system (Fig. 18): for a first read of information from a DDR memory [24, 26], activating termination loads [452] on said memory controller's side [31] of a data

bus [28] between said memory controller [31] and said DDR memory [24, 26]; for a write of information into said DDR memory, deactivating said termination loads (See Page 2, lines 12 – 14 of paragraph 0032); and, for a second read of information from said DDR memory, activating said termination loads (this is inherent to the method of Greff et al. as discussed above, because Greff et al. taught the terminal loads [452] is activated for each and every read operations. Therefore, the termination loads 452 is activated for second read operation, or third read operation, or fourth read operation and so on).

Regarding independent claim 32, Greff et al. discloses an apparatus, comprising: a computing system (Fig. 18) comprising: a memory controller [31] comprising a data bus [28] termination loads [452], said data bus coupled to a DDR memory [24, 26], said termination loads [452] coupled to an output [39] of memory controller logic circuitry [31], said memory controller logic circuitry to drive said output to place said termination loads in an activated state during a read phase of said DDR memory and to place said termination loads in a deactivated state during a write phase of said DDR memory.

Regarding independent claim 39, Fig. 18 of Greef et al. discloses a machine readable medium having stored thereon a description of a design for a memory controller (31), the memory controller comprising: a data bus [28] termination loads [452], said data bus to couple to a memory [24, 26], said termination loads [452] coupled to an output of memory controller logic circuitry [31], said memory controller logic circuitry to drive said output to place said termination loads in an activated state

during a memory read phase and to place said termination loads in a deactivated state during a memory write phase (See Page 2, lines 12 – 14 of paragraph 0032).

Allowable Subject Matter

6. Claims 2 – 12, 14 – 19, 21 – 31, 33 – 38, and 40 – 44 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claims 2 and 21, in addition to other elements in the respective claim, the prior art does not teach or suggest " the memory controller, activating said termination loads for said first read of information as a consequence of a first signal indication of a first clock cycle of a plurality of consecutive clock cycles, a memory read phase being performed by said memory controller over said plurality of clock cycles, said first read of information occurring within said plurality of clock cycles".

With respect to claims 8 and 27, in addition to other elements in the respective claim, the prior art does not teach or suggest "wherein said deactivating occurs within a clock cycle that immediately follows a last clock cycle of a plurality of clock cycles that mark a read phase within which said first read of information occurs".

With respect to claims 9 and 28, in addition to other elements in the respective claim, the prior art does not teach or suggest "wherein said activating occurs in response to an edge that appears in a chip select (CS) signal".

With respect to claims 10 and 29, in addition to other elements in the respective claim, the prior art does not teach or suggest "asserting a bypass control signal to activate said termination loads while information is being read from said memory".

With respect to claims 11 and 30, in addition to other elements in the respective claim, the prior art does not teach or suggest "asserting an enable control signal and not asserting a bypass control signal so as to permit said activating".

With respect to claims 12 and 31, in addition to other elements in the respective claim, the prior art does not teach or suggest "for said first read of information from a memory, activating a termination load on said memory controller's side of a data strobe wire between said memory controller and said memory; for said write of information into said memory, deactivating said data strobe wires said termination load; and, for said second read of information from said memory, activating said data strobe wire termination load".

With respect to claims 14, 33, and 40, in addition to other elements in the respective claim, the prior art does not teach or suggest "wherein said logic circuitry comprises a latch, said latch to latch a first value, said first value to place said termination loads in said activated state, said latch to also provide a second value, said second value to place said termination loads in said deactivated state".

With respect to claims 16, 35 and 42, in addition to other elements in the respective claim, the prior art does not teach or suggest "wherein said logic circuitry further comprises a logic gate between said output and a bypass input to said logic

circuitry, said logic gate to place said termination loads into one of said states when said bypass input is asserted".

With respect to claims 17, 36, and 43, in addition to other elements in the respective claim, the prior art does not teach or suggest "wherein said logic circuitry further comprises a second logic gate between said output and a tweak input, said second logic gate to place said termination loads into said activated state based upon a first tweak input value, said second logic gate to place said termination loads into said deactivated state based upon a second tweak input value".

With respect to claims 18, 37, and 44, in addition to other elements in the respective claim, the prior art does not teach or suggest "wherein said logic circuitry further comprises a chain of delay elements to allow a delay to be programmed, said delay imposed between a first moment when a memory read phase is indicated and a second following moment when said termination loads are placed into said activated state".

With respect to claims 19 and 38, in addition to other elements in the respective claim, the prior art does not teach or suggest "wherein said memory controller further comprises a data strobe wire's termination load, said data strobe wire to couple to said memory, said data strobe wire's termination load coupled to said output of said memory controller logic circuitry, said memory controller logic circuitry to drive said output to place said data strobe wire's termination load in an activated state during said memory read phase and to place said data strobe's termination load in a deactivated state during said memory write phase".

Prior art

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Janzen et al.	Patent No. US 6,538,951 B1	Date of Patent: Mar. 25, 2003
Cassetti et al.	Patent No. 5,781,802	Date of Patent: Jul. 14, 1998
Kible	Patent No. 4,400,801	Date of Patent: Aug. 23, 1983

Contact Information

8. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.

Dang Nguyen 12/21/2004

12/21/04

RICHARD ELMS
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